COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF MICHIGAN

DISSERTATION DEFENSE

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Systems and Debugging Supports for Hardware Designs

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3725 Beyster
Hybrid – Zoom

ABSTRACT: The development and deployment of hardware and software have traditionally been quite distinct. Software benefits from an agile development cycle, aided by a wide array of debugging tools---such as step-wise debuggers, logging frameworks, and both static and dynamic analyses---and is further simplified by its integration with multiple layers of systems---such as hypervisors, operating systems, and libraries. Unfortunately, such debugging and systems supports are less explored and usually not available in the hardware domain.

Accordingly, this dissertation research focuses on exploring and developing systems and debugging supports tailored for modern hardware designs. It presents several studies and systems that demonstrate the feasibility and benefits of these supports. In particular, it first introduces Optimus, a hypervisor designed for shared-memory FPGA platforms. Optimus implements both spatial and temporal multiplexing, allowing an FPGA to be shared in different ways in a cloud environment. Additionally, this dissertation presents a comprehensive study on bugs in FPGA-based hardware designs, and proposes a set of specialized debugging tools to assist the localization of these bugs. The final part of this dissertation addresses the challenge of aging-related silent data corruptions (SDCs) increasingly observed in data centers. It introduces Vega, a bottom-up approach that constructs concise tests for SDC detection by examining the hardware's implementation details, therefore allowing these errors to be effectively and efficiently detected.

CHAIR: Prof. Baris Kasikci